Abstract

Certain embodiments relate to semiconductor devices having an improved dielectric strength and methods for manufacturing the same. A semiconductor device 1000 may have a field effect transistor 100. The field effect transistor 100 includes a gate dielectric layer 30, a source region 32 and a drain region 34. A first semi-recessed LOCOS layer 40 may be formed between the gate dielectric layer 30 and the drain region 34. A second semi-recessed LOCOS layer 50 may be formed between the gate dielectric layer 30 and the source region 32. A first offset impurity layer 42 may be formed below the first semi-recessed LOCOS layer 40. A second offset impurity layer 52 may be formed below the second semi-recessed LOCOS layer 50